Carbon Nanotubes Bumps for Off-Chip Electrical Interconnects

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Despite many challenges, carbon nanotubes (CNTs) is one of the key emerging materials for potential use in off-chip electrical interconnects. Off-chip interconnects processes are generally located at the backend packaging level, and its feature sizes are considerable large and have feature sizes in the microns levels. Typically off-chip interconnects methodology include flip chip and through silicon vias (TSVs) technology. Under More-than-Moore law, the significant of function integration (such as RF) and downscaling of packages dimensions will be one of the key future trends. However, at the same time of fulfilling the scaling trends, conventional metals are facing the limitations of electro-migration, scattering and skin depth effect at radio frequency. Hence compatible design integration and characterization of CNT at both DC and radio frequency must be explored.

The design integration processes to fabricate CNT bumps for flip chip application have been successfully demonstrated. By interconnecting CNT bumps to CNT bumps using a flip chip methodology, electrical conduction through CNTs to CNTs have been achieved [1]. Initially measurements at the DC and high frequency (up to 40 GHz) have also shown the potential of our fabrication methodology. In this work, the densities of the CNT bumps, barrier layers will be varied and addressed. It is believed that the densities of the CNT play a significant role to reduce the overall bump resistivity. A higher conductive and thinner barrier will also help to reduce the contact resistance of the CNT bumps. Different bumps designs will also be discussed. Characterization using DC 4-point probe and RF measurements using vector network analyzer will be demonstrated. With better designs, the performances of CNT bumps can be further improve and become closer to meet/be better than the current metal.